ABSTRACT OF THE DISCLOSURE

SYSTEM AND METHOD FOR ENCODING AND DECODING ARCHITECTURE REGISTERS

A system and method to extend the number of architecturally visible registers in a processor while preserving the number of bits of the instruction encoding. The system comprises: an indirection table that encodes register patterns for the registers used in an instruction; instructions to load and store such table entries; a mechanism to identify instructions that use the indirection table; and a mechanism to identify a set of bits in instructions that are used to index into the indirection table. According to another embodiment, a method of encoding registers in a computer instruction comprises constructing a table having a plurality of entries. Each entry specifies a combination of a plurality of registers. The method also comprises generating an instruction having a reference to one of the entries in the table. The method then comprises accessing the plurality of registers specified by the referenced table entry. The method further comprises merging said number of registers into an expanded instruction that is used for remaining stages of instruction processing.

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